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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,529	04/13/2004	Bo Jin	CD03021	4879

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EXAMINER	
LAM, DAVID	

ART UNIT	PAPER NUMBER
2827	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,529	JIN ET AL.	
	Examiner	Art Unit	
	David Lam	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 21-23* is/are rejected.

7)☒ Claim(s) *6-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to amendment file on 11/17/06.

   - Claims 4 and 8-20 have been cancelled.
   - Claims 21-23 are newly added.
   - Claims 1-3, 5-7, and 21-23 are pending.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-3, 5, 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Hashimoto et al. (5,780,910).

Regarding to claims 1-3, Hashimoto et al. disclose a memory cell comprising: a first node (A) for storing a first potential; a second node (B) node for storing a second potential; transistor gates formed a gate layer (8 or 11); a capacitor (C) having plates coupled between the first node and second node (See at least Fig. 4), a portion of one plate (16, 19, 41, 42, 61 or 62) of the capacitor comprising a first interconnect wiring (16 and 19; 41 and 42, or 61 and 62 utilized as wiring lines or L1, L2) formed over the gate layer that includes a plurality of conductive layers (16, 19; 41, 42, or 61, 62) that electrically interconnects circuit components of the memory cell; a first inverter (Qp1, Qd1) having an input coupled to the first node and an output coupled to the second node; a second inverter (Qp2, Qd2) having an input coupled to second node and an output coupled to the first node; the first node stores a true data value and the second node stores a complementary data value; a first access transistor (Qt1) coupled to the first node; and a second access transistor (Qt2) coupled to the second node. *See at least Figs. 3-4, 34, 36, 61, for example of Col. 11, lines 24-64, Cols. 20-21, lines 1-67, 1-23, respectively, Cols. 28-29, lines 61-67, 1-67, respectively, and the related disclosure.*

Regarding to claims 5, Hashimoto et al. disclose wherein the first conductive interconnect wiring includes a plurality of separate portions (see at least Fig. 3, 12, 14, 16, 19), bottom conductive layer (16, 41 or 61), a dielectric layer (18) formed over the bottom conductive layer, and a top conductive layer (19, 42, 62) formed over the dielectric layer, the top conductive layer forming at least a portion of the first plate of the capacitor

With respect to claims 21-22, Hashimoto et al. further disclose wherein the gate layer (8 or 11) is not physical contact with a drain of any transistor of the memory cell; a first portion of the interconnect wiring is in physical contact with the drains of a first and second transistors (node A) of the memory cell; a second interconnect wiring, separated from the first portion, is in physical contact with the drains of a third and fourth transistor (node B) of the memory cell. *See at least Fig. 4, for example of Col. 11, lines 24-64, and the related disclosure.*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claim 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al. (5,780,910) in view of Nagai (6,104,053).

Hashimoto et al. disclose a memory cell comprising: a first node (A) for storing a first potential; a second node (B) node for storing a second potential; transistor gates formed a gate layer (8 or 11); a capacitor (C) having first plate (19 or 42 or 61) coupled to the first data node, a second plate (16 or 41 or 62) coupled to the second data note, the first and second plates comprising portion of a interconnect layer electrically connects terminals of the memory cells. *See at least Figs. 3-4, 34, 36, 61, for example of Col. 11, lines 24-64, Cols. 20-21, lines 1-67, 1-23, respectively, Cols. 28-29, lines 61-67, 1-67, respectively, and the related disclosure.*

Nagai discloses a semiconductor memory device comprising a first plate (electrode 11) of the capacitors; a second plate (electrode 20) of the capacitors; a third plate (electrode 40) separated from the first and second plates by a capacitor dielectric (42). *See at least Fig. 1, 34, for example of Cols. 11, lines l-47 and the related disclosure.*

Hashimoto et al. fail to specify a third plate separated from the first and second plates by a capacitor dielectric. It would have been obvious to one having ordinary skill in the art at the time of the invention the provide a third plate separated from the first and second plates by a capacitor dielectric of Hashimoto capacitor as taught by Nagai in order to form a constant capacitance, highly reliable capacitors.

Response to Arguments

Applicant's arguments filed on 11/17/06 have been fully considered but they are not persuasive.

With respect to Applicant's arguments on pages 7-12 of the remarks, for example of "Hashimoto et al. (5,780,910) fails to disclose a plurality of conductive layers (line 23 of the remarks); the capacitor do not electrically connect any device of a memory cell (lines 12-13 of the remarks); " The Examiner disagrees with this statement; Hashimoto et al. (5,780,910) disclose a plurality of conductive layers (See at least Cols. 2-3, lines 31-67, lines1-32, respectively); and the capacitor is electrically connect to device of the memory cell (See at least Figs. 3-4). Accordingly, the rejection set forth above is proper.

Applicant's arguments with respect to newly added claim 23 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

5. Claims 6-7 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach all the elements as applied to claim 5 and further comprising the limitation of claim 6.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Lam whose telephone number is 571-272-1782. The examiner can normally be reached on 6:00 – 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Lam

January 26, 2007

DAVID LAM
PRIMARY EXAMINER